

REMARKS

Claims 1-26 and 49-55 are currently in the application for further prosecution. By this amendment, Claims 1, 22, 49, 53 and 55 have been amended. Claims 56- 57 have been added.

Claim Rejection § 103

Claims 1, 7-11, 13-15, 21-26, 49 and 52-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 7,142,731 ("Toi") in view of U.S. Patent No. 5,910,733 ("Bertolet") and further in view of U.S. Patent No. 6,507,211 B1 ("Schultz").

Claims 2-6, 12 and 50-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 7,142,731 ("Toi") and U.S. Patent No. 5,910,733 ("Bertolet") in view of U.S. Patent No. 6,507,211 ("Schultz") and further in view of U.S. Patent No. 6,778,212 ("Deng").

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 7,142,731 ("Toi") and U.S. Patent No. 5,910,733 ("Bertolet") in view of U.S. Patent No. 6,507,211 ("Schultz") and further in view of U.S. Patent No. 5,754,227 ("Fukuoka").

Interview Summary

The Applicant notes with appreciation the interview conducted with Examiners Hernandez and Tran on April 9, 2008. In the Interview, the Applicant reviewed the features of the claims in view of the cited references. The Examiners indicated that the terms "computational elements" and "interconnection network" could be further defined to distinguish the cited references. Applicant agreed to consider further amendments of these claim elements.

As explained in the interview, the present invention relates to image processing that takes advantage of the use of heterogeneous computational units composed of multiple computational elements that may be rapidly reconfigured via an interconnection network. The Office Action acknowledges that Toi does not disclose heterogeneous computational elements or an

interconnection network. The Office Action has combined Toi with Bertolet which allegedly discloses heterogeneous computational elements and Schultz which allegedly discloses an interconnection network.

The Amended Claims and the Cited References

As explained in the interview, Bertolet does not disclose heterogeneous computational units having a plurality of computational elements. The “heterogeneous elements” in Bertolet are the actual circuit elements that comprise a computational unit in the form of an FPGA. Certain integrated circuits that make up the basic computational element (FPGA) such as logic cells, interconnect, repeaters, etc. are disparate in nature. Col. 2, ll. 14-18. However, the basic computational unit, an FPGA, is homogeneous as it relates to other basic computational units which are all identical computational units (FPGAs). The amended claims are now directed toward computational units that have different (“heterogeneous”) architectures in relation to other computational units in the same apparatus. As Bertolet explains, “at the device level, FPGAs are heterogeneous in nature, i.e., they are not comprised of a pure repetition of a single type of circuit. FPGAs rather comprise a multitude of different circuit types, **which when viewed at higher levels of circuit type grouping, may be considered repetitive or scaleable.** Col. 1, l. 66 to Col. 2, l. 4 (emphasis added). The computational units themselves (e.g., the FPGAs) are in fact homogeneous in Bertolet and therefore similar to those in Toi.

As also explained in the interview, Schultz does not disclose a network as Schultz is directed toward a grid structure that allows an individual FPGA to be configured by activating the correct address lines. Schultz therefore has a grid structure which is not a network configuration that enables different simultaneous configuration and reconfiguration of different interconnections between the computational elements. Further, Schultz does not disclose the use

of the network for both configuration data such as commands to change the interconnections and image data itself.

Applicant has amended claims 1, 49 and 55 to require that a plurality of heterogeneous computational units include a first computational unit with a first architecture having a first plurality of computational elements and a second computational unit with a second different architecture with a plurality of computational elements. The computational elements all include algorithmic logic, a data input and a data output. Amended dependent claims 22 and 53 further define the different functions of algorithmic logic of the computational elements. The amended claims are now patentable over the combination of Toi, Bertolet and Schultze. Such a combination does not disclose heterogeneous computational units because the FPGAs in Bertolet are the same computational units. The “heterogeneous” electronic circuit elements described in Bertolet are not computational units having different computational elements. As explained above, the computational unit level (cell) in Bertolet are actually prior art FPGAs having computing elements that are the same for each cell.

Applicant has also amended claims 1, 49 and 55 by requiring that the interconnection network “simultaneously in response to different configuration information” provide to the respective interconnections between some and others of the plurality of computational elements. The configuration information for different interconnections for different computational elements cannot be simultaneously provided in Schultze as now required by these claims. As explained above, Schultze’s grid arrangement only allows the changing of one interconnection at a time, simultaneous provision of configuration information to different interconnections is impossible because each row and address must be strobed one at a time.

Similarly, Applicant is adding new claim 56 that is allowable over the cited references for the same reasons as noted above.

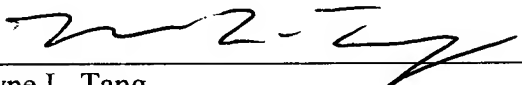
Conclusion

It is Applicant's belief that all of the claims are now in condition for allowance and actions towards that effect is respectfully requested.

If there are any matters which may be resolved or clarified through a telephone interview, the Examiner is respectfully requested to contact the undersigned attorney at the number indicated.

Respectfully submitted,

Date: August 14, 2008



Wayne L. Tang
Reg. No. 36,028
NIXON PEABODY LLP
401 9th Street N.W. Suite 900
Washington, D.C. 20004
(312) 425-3900
Attorney for Applicants